John Peck

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PROFESSIONAL SUMMARY

John Peck is an expert in complex constrained random design verification and board validation environments. He has developed and performed verification of memory controllers (SDRAM, DDR), on-chip interconnect networks, and processor instruction set architectures (ISAs). He is knowledgeable about performance modeling and architectural validation of network processors and has designed high throughput software applications including search indexers and text extractors. He holds a bachelor's degree in Computer Engineering from Carnegie Mellon University and a master's degree in Computer Science from the University of California, Los Angeles.

EXPERIENCE

11/2012 – present: Zeidman Consulting - Research Engineer

- Reads patents to understand infringement and validity issues
- Examines schematics for determining patent infringement
- Examines HDL code (e.g., Verilog and VHDL) for determining patent infringement
- Examines software source code for determining patent infringement
- Writes expert reports

1/2008 – Present: Bay2Sierra Silicon Services - Research Engineer

- Patent reviews
- Performance analysis and modeling
- ASIC/FPGA design verification, architecture, and design
- Complex SOC platform: IP design vetting/integration, and integration-level verification
- Design verification/validation of FPGA designs implemented in PCIe platform
- Design of hardware and software for high throughput applications
- Development of electronic design automation tools (EDA)
- Development of OpenSSL crypto-engine software integration for hardware devices including Atmel ATECC508A

12/2003 – 12/2007: Kazeon Systems - Senior Member of Technical Staff, Office of the CTO

- Responsible for system hardware and set performance goals and expectations
- Managed technical engagement with vendors and customers
- Designed high throughput search indexer based on Lucene
- Designed and implemented vectorized algorithms on x86 processors for text extraction at 1Gbps line rate throughputs

08/1999 – 12/2003: Redback Networks (formerly with Siara Systems) - Senior Member of Technical Staff

- Network processors
- Architectural validation using performance-modeling methodologies: Implemented custom cycle-based model in C++.
- Functional verification of processor ISA, inter-chip interface blocks, performance measurement counters.
- RTL design of DDR SDRAM memory controller optimized for high throughput.

10/1997 – 08/1999: Advanced Micro Devices, Inc.

- Senior design engineer, Platforms Products Division: K7 Northbridge chipset design team responsibilities include: Design, writing RTL, verification, synthesis, and hand placement. Wrote verification testbench for SDRAM memory controller, implemented RTL/verified GART virtual address translation block, enhanced AGP block for 4x operation.

1994 – 1997: University of California - Graduate Student Researcher

- Research on Supercomputer Supernetwork joint work of UCLA and the Jet Propulsion Laboratory (ARPA funded project)
- Co-Designed/Co-implemented Optical Channel Interface Gateway for Myrinet Network.

02/1996 – 06/1997: Activision Studios - Consultant/Software Engineer

- Video Game Software Engineer for Win95 Platform
- Product implemented is entitled “Dark Reign: The Future of War”
- Video Game Software Engineer for PC Platform. Product implemented is entitled “Mechwarrior 2: Mercenaries.”

05/1995 – 07/1995: Software Engineer Redline Games - contractor to Activision Studios

- Video Game Software Engineer for PC platform and SNES platform (Nintendo game machine)
- Product implemented is entitled “Mechwarrior 2: 31st Century Combat.”
- Product implemented was entitled “Pitfall: The Mayan Adventure."

06/1994 – 08/1994: Redline Games - contractor to Activision Studios

- Video Game Software Engineer for SNES platform (Nintendo game machine)
- Product implemented was entitled “Pitfall: The Mayan Adventure."

06/1992 – 08/1992: NCR Corporation E&M Atlanta - Software Engineer

- OS Development group
- Programmer / Analyst device driver development DOS 5.0.

06/1991 – 08/1991: Transarc Corporation - Software Engineer

- Product Support
- Distributed system testing and debugging.

1988 – 1993: Foxfire Technologies Corporation - Software Engineer

- Analysis and Computer Programming
- Inquiry system for real time shop floor control, Controller for real time data collection, Capacity planning and scheduling system, Finished goods inventory system, Shipping system, Control software for Rapistan automated conveyor sortation system, Router for real time data collection.

LEGAL CONSULTING

1/2016 – 6/2016: Verasonics v. Alpinion Medical Systems

Law Firm: Davis Wright Tremaine
Client: Verasonics
Venue: American Arbitration Association, International Centre for Dispute Resolution
Case: 01-15-0002-9484

- Alleged trade secret theft of software for an ultrasound research platform.
- Compared software source code using CodeSuite.
- Assisted with the writing of a declaration and an expert report.

2/2015 – 1/2016: NNG, Kft. v. Ava Enterprises, Inc.

Law Firm: Lewis Roca Rothgerber Christie LLP
Client: NNG, Kft
Court: U.S. District Court, Central District of California
Case: 2:2014-CV-00220

- Alleged copyright infringement

1/2015 – 6/2015: NVidia Corporation vs. Samsung Electronics, Qualcomm Inc.

Law Firm: Orrick, Herrington & Sutcliffe
Client: NVidia Corporation
Court: U.S. International Trade Commission
Case: Inv. No. 337-TA-932

- Alleged patent infringement of GPU integrated circuits
- Examined HDL code
- Wrote expert report pertaining to source code analysis

11/2012 – 5/2014: Intellectual Ventures v. Altera, Microsemi, Lattice Semiconductor, and Xilinx

Law Firm: Desmarais LLP
Client: Intellectual Ventures
Court: U.S. District Court, District of Delaware
Case: C.A. No. 10-1065-LPS

- Alleged patent infringement of FPGA and ASIC integrated circuits
- Examined schematics and Verilog code.
- Assisted with writing expert reports.

EDUCATION

Masters Degree in Computer Science, University of California, Los Angeles, March 1995

Bachelor of Science in Computer Engineering, Carnegie Mellon University, May 1992

PUBLICATIONS

1. J. Cong, J. Peck, et al., "The Supercomputer Supernet Testbed: A WDM-based Supercomputer Interconnect," *Journal of Lightwave Technology*, 1996.
2. J. Cong, J. Peck, Y. Ding, "RASP: A General Logic Synthesis Systems for SRAM-based FPGAs," *ACM/IEEE Inter. Symposium on FPGAs*, 1996.
3. J. Cong, J. Peck, et al., "The Supercomputer Supernet (SSN): A High-Speed Electro-Optic Campus and Metropolitan Network," *Society of Photo-Optical Instrumentation Engineers*, 1996.
4. J. Cong, J. Peck, "On Acceleration of Logic Synthesis Algorithms using FPGA-based Reconfigurable Coprocessors," *IEEE Inter. Symposium on FPGAs for Custom Computing Machines*, 1997.

PATENTS

1. Peck, John; Davis, Gregory; Huynh Quoc, "Serial peripheral interface," U.S. Patent 8,589,717.
2. Novak; Stephen T., Peck, Jr.; John C., Waldron; Scott, "Method and apparatus for optimizing memory performance with opportunistic refreshing," U.S. Patent 6,046,952.
3. Novak; Stephen T., Peck, Jr.; John C, Waldron; Scott, "Method and apparatus for optimizing memory performance with opportunistic refreshing," U.S. Patent 6,147,921.
4. Novak; Stephen T., Waldron; Scott, Peck, Jr.; John C., "Queue-based memory controller," U.S. Patent 6,295,586.
5. Novak; Stephen T., Peck, Jr.; John C., "Method and apparatus for optimizing memory performance with opportunistic pre-charging," U.S. Patent 6,360,305.
6. Novak; Stephen T., Peck, Jr.; John C., "Queue-based control mechanism for queue-based memory controller," U.S. Patent 6,393,531.
7. Novak; Stephen T., Waldron; Scott, Peck, Jr.; John C., "Queue-based memory controller," U.S. Patent 6,496,906.
8. Peck, Jr.; John C., Subramanian; Sridhar P., "Optimized static sliding-window for ACK sampling," U.S. Patent 6,601,182.

9. Peck, Jr.; John C., Subramanian; Sridhar P., Waldron; Scott, “Optimizing the translation of virtual addresses into physical addresses using a pipeline implementation for least recently used pointer,” U.S. Patent 6,686,920.
10. Peck, Jr.; John C., Subramanian; Sridhar P., Waldron; Scott, “Distributed translation look-aside buffers for graphics address remapping table,” U.S. Patent 6,741,258.

SPECIAL KNOWLEDGE AND SKILLS

- FPGAs, ASICs, SoCs, Processors, Chipsets
- HDL-Software Interfaces:
    - Programming Language Interface (PLI)
    - SystemVerilog Direct Programming Interface (DPI)
    - Verilog Procedural Interface (VPI)
- Operating systems:
    - Linux
    - UNIX
    - Windows
- Programming languages:
    - assembly language, including x86 vector programming
    - C
    - C++
    - Perl
    - Python, including embedded w/SWIG
    - Java
- Scripting languages:
    - Bash
    - Csh
- Synopsys Design Compiler (DC)
- SystemVerilog
- Verilog
- Verification methodologies:
    - Universal Verification Methodology (UVM)

CERTIFICATIONS AND COURSE TRAINING

- Code Suite Certified by SAFE Corporation
- Computer Forensics CNIT 121
- Ethical Hacking and Network Defense CNIT 123
- Intellectual Property PLS 13